WHAT IS CLAIMED IS

1. A method comprising:

storing a plurality of branch marker bits, wherein each bit of said plurality of bits:

corresponds to a different byte range within a group of contiguous instruction bytes; and

indicates whether a predicted branch instruction ends within the corresponding byte range;

selecting one of said plurality of branch marker bits in response to receiving a fetch address; and

utilizing said selected branch marker bit to make a prediction.

2. The method of claim 1, further comprising storing branch prediction information corresponding to said plurality of branch marker bits, wherein said information comprises a plurality of entries each of which includes information regarding predicted taken branches.

3. The method of claim 2, wherein each of said entries indicates a type of branch instruction.

4. The method of claim 3, wherein each of said entries further indicates a past behavior of a branch.

5. The method of claim 1, further comprising determining whether any of said branch marker bits occurring before said fetch address indicates a predicted branch instruction.

6. The method of claim 5, further comprising storing branch prediction information corresponding to said plurality of branch marker bits, wherein said information comprises a plurality of entries each of which includes information regarding a predicted branch.

7. The method of claim 6, wherein the number of said plurality of entries is equal to a maximum number of branches which may be indicated as predicted by said branch marker bits at one time.

8. The method of claim 6, further comprising selecting an entry of said entries in response to detecting said selected bit is indicative of a predicted branch, wherein said selected entry is determined by a position of said selected branch marker bit relative to other bits of said branch marker bits which are also indicative of predicted branches.

9. The method as recited in claim 1, wherein selecting one of said plurality of bits comprises decoding a plurality of least significant bits of said fetch address.

10. The method as recited in claim 1, wherein the largest range of said different byte ranges includes a number of bytes equal to a number of bytes within a shortest branch instruction exclusive of a return instruction.

11. The method as recited in claim 1, wherein selecting said branch marker bit comprises identifying a first branch marker bit which corresponds to an address at or after said fetch address.

12. The method of as recited in claim 1, wherein each of said branch marker bits further indicates whether a corresponding branch instruction has previously been mispredicted.

13. A branch prediction mechanism comprising:

a branch prediction storage coupled to receive a fetch address, wherein said branch prediction storage is configured to store a plurality of branch marker bits, wherein each bit of said bits:

corresponds to a different byte range of a group of contiguous instruction bytes; and

indicates whether a predicted branch instruction ends within the corresponding byte range;

a control unit configured to:

select one of said plurality of branch marker bits in response to receiving said fetch address; and

utilize said selected branch marker bit to make a prediction.

14. The branch prediction mechanism of claim 13, wherein said mechanism is further configured to store branch prediction information corresponding to said plurality of branch marker bits, wherein said information comprises a plurality of entries each of which includes information regarding predicted branches.

15. The branch prediction mechanism of claim 14, wherein each of said entries indicates a type of branch instruction.

16. The branch prediction mechanism of claim 15, wherein each of said entries further indicates a past behavior of a branch.

17. The branch prediction mechanism of claim 13, wherein said control unit is further configured to determine whether any of said branch marker bits occurring before said fetch address indicates a predicted branch instruction.

18. The branch prediction mechanism of claim 17, wherein said mechanism is further configured to store branch prediction information corresponding to said plurality of branch marker bits, wherein said information comprises a plurality of entries each of which includes information regarding a predicted branch.

19. The branch prediction mechanism of claim 18, wherein the number of said plurality of entries is equal to a maximum number of branches which may be indicated as predicted by said branch marker bits at one time.

20. The branch prediction mechanism of claim 18, wherein when said selected bit is indicative of a predicted branch, said mechanism is further configured to:

determine a position of said selected bit relative to other bits of said branch marker bits which are also indicative of predicted branches; and

determine which of said plurality of entries corresponds to said selected bit.

21. The branch prediction mechanism of claim 18, wherein said mechanism is further configured to select an entry of said entries in response to detecting said selected bit is indicative of a predicted branch, wherein said selected entry is determined by a position of said selected branch marker bit relative to other bits of said branch marker bits which are also indicative of predicted branches.

22. The branch prediction mechanism as recited in claim 13, wherein selecting one of said plurality of bits comprises decoding a plurality of least significant bits of said fetch address.

23. The branch prediction mechanism as recited in claim 13, wherein the largest range of said different byte ranges includes a number of bytes equal to a number of bytes within a shortest branch instruction exclusive of a return instruction.

24. The branch prediction mechanism as recited in claim 13, wherein said control unit is further configured to identify a first branch marker bit which corresponds to an address at or after said fetch address.

25. The branch prediction mechanism as recited in claim 13, wherein each of said branch marker bits further indicates whether a corresponding branch instruction has previously been mispredicted.

26. A microprocessor comprising:

an instruction cache coupled to receive a fetch address and to provide a group of contiguous instruction bytes in response to said fetch address; and

a branch prediction unit coupled to receive said fetch address concurrently with said instruction cache, wherein said branch prediction unit is configured to:

store a plurality of branch marker bits, wherein each bit of said bits:

corresponds to a different byte range of a group of contiguous instruction bytes; and

indicates whether a predicted branch instruction ends within the corresponding byte range;

select one of said plurality of branch marker bits in response to receiving said fetch address; and

utilize said selected branch marker bit to make a prediction.

27. The microprocessor of claim 26, wherein said branch prediction unit is further configured to store branch prediction information corresponding to said plurality of branch marker bits, wherein said information comprises a plurality of entries each of which includes information regarding a predicted branch.

28. The microprocessor of claim 27, wherein said branch prediction unit is further configured to:

determine a position of said selected bit relative to other bits of said branch marker bits; and

determine which of said plurality of entries corresponds to said selected bit.

29. The microprocessor of claim 26, wherein said branch prediction unit is further configured to identify a first branch marker bit which corresponds to an address at or after said fetch address.